# Application Note

## Application Note

### AN1151

### APM32F072 Series Application Note

**Version: V1.0**

# 1 Introduction

This application note provides precautions to be taken when using the APM32F072 series.

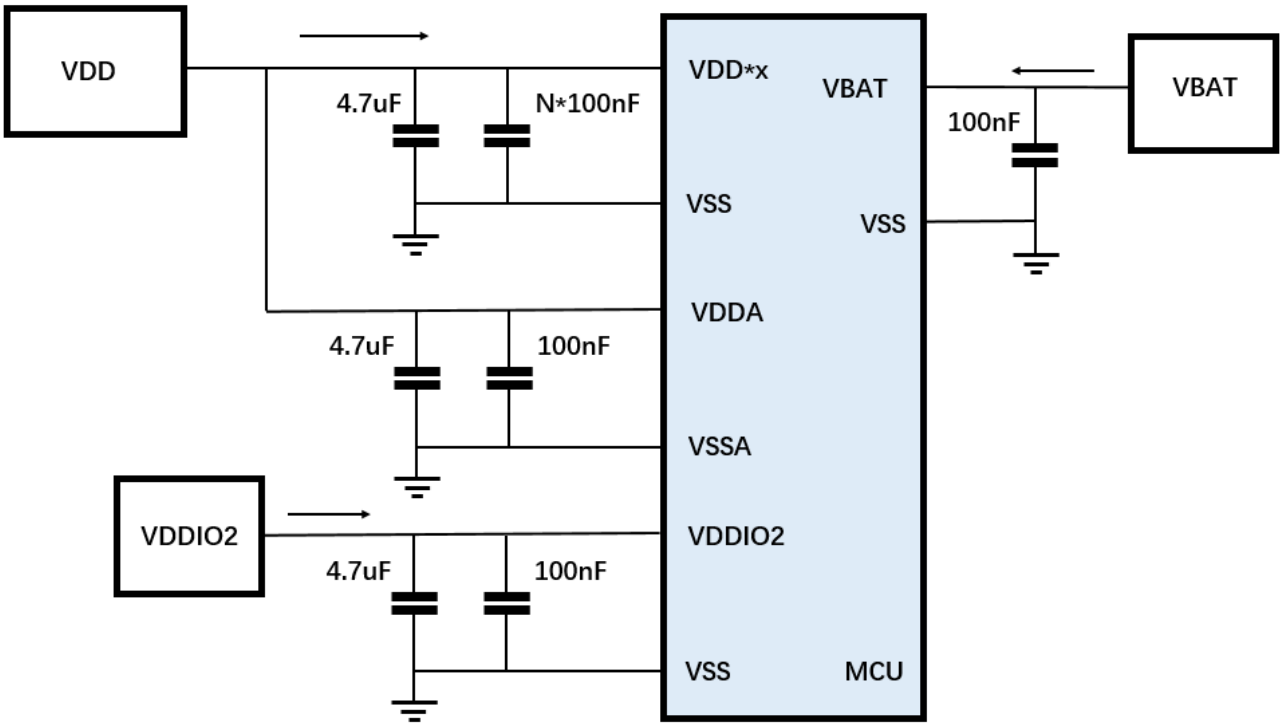
# Contents

# 2 Note to Hardware Application Design

## 2.1 Design of MCU Filter Capacitor

The chip power port needs to be connected in parallel to large and small filter capacitors. The effectiveness of capacitors depends on the optimal placement and connection type. PCB layout requires star-shaped wiring, and it is important to note that the external power supply passes through large and small capacitors and then connects to the chip. The large and small filter capacitors should be placed as close to the chip as possible within 4mm. The capacitor design reference is shown in Figure 1.

Figure 1 Capacitor Design




The VBAT pin can be connected to an external battery (1.8V<3.6V). If there is no external battery, an external 100nF ceramic capacitor should be connected to the VDD power supply together.

VDD must be connected to VDD power supply of an external capacitor (N 100nF ceramic capacitor(s) and a tantalum capacitor not less than 4.7μF). VDD*x represents that the number of VDD is x.

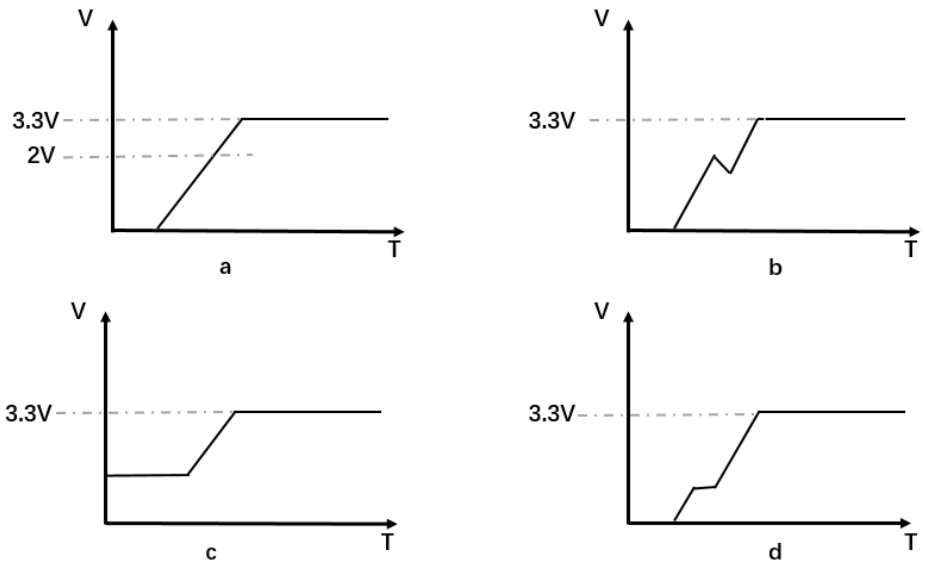
VDDA and VDD are connected together to power the ADC, DAC, HSICLK, LSICLK, PLL and reset module. When ADC is used, VDDA is greater than or equal ato 2.4V. VDDA and VSSA must be connected to VDD and VSS respectively.

The VDDIO2 pin supplies power to some IO.

## 2.2 Precautions for MCU Power Supply Ramp Rate

The MCU's power supply ramp rate should meet the required maximum and minimum value limits, namely greater than 0.5V/min and less than 100V/ms respectively. The power on/down time from 0V to 3V requires at least 30us. Too high or too low power-on rate may cause the MCU to fail to work normally; MCU needs to be powered down to below 300mV before being powered on again, and the above time must meet the requirements within the full temperature range. The power-on startup waveform needs to meet the waveform a in Figure 2, while the other three waveforms are incorrect.

Figure 2 Power-on Waveform




## 2.3 The peripheral module uses VDD and VSS

When MCU is used to control the power supply or power-on process of external modules, too high power-on rate should be avoided to prevent the problem of VDD voltage being pulled down due to sudden current changes. To ensure stable operation of the system and protect the circuit from potential damage, it is recommended to adopt appropriate delay measures for steady power supply conversion.

Appropriate buffer elements such as capacitors and resistors can be added to the MCU power supply end to buffer the fast power-on and power-down speed of the power supply, so that voltage dip will not be caused to VDD due to instantaneous high current demand. If sudden dip is caused for this reason, the drop speed must also meet the requirements of the MCU's power supply ramp rate. In the scenarios shown in Figures 3 and 4, in order to avoid power fluctuation, connect a buffer circuit (composed of MOS transistor, capacitor, and resistor) in series on the control circuit, or connect a 10R resistor in series and a capacitor of 10uF and above on the circuit, to form a fast power-on/power drop protection circuit. If the capacitance is large enough, the power down will be slow and the power-down magnitude can be very small.

Figure 3 Power Supply of IO Control Peripheral Module

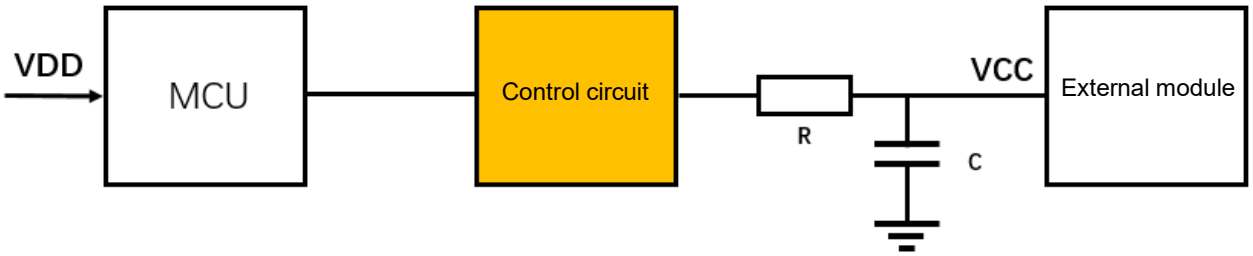
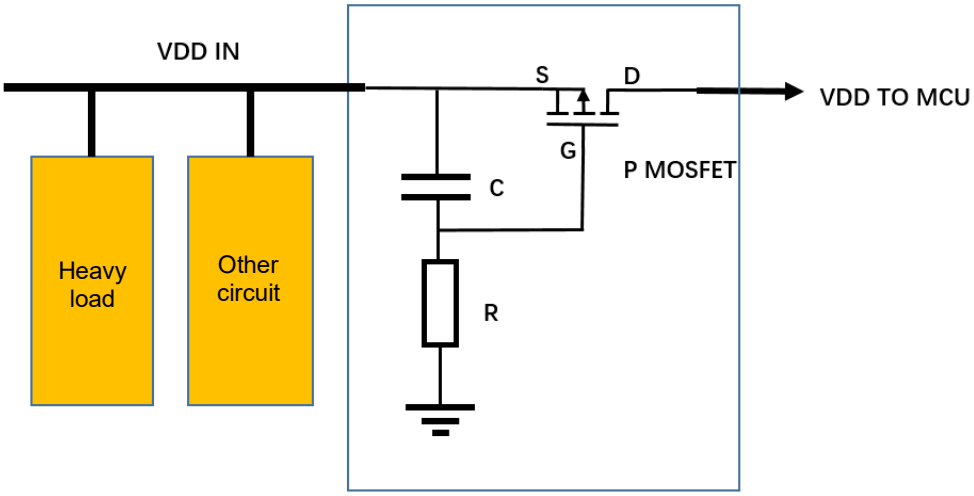



Figure 4 Shared Power Supply for Peripherals




## 2.4 External and High-frequency Signals

Attention should be paid to checking whether an instantaneous increase in load may be caused by zero-crossing signals, relay signals, AC loads, etc. The load impact can be mitigated by bypass capacitors.

For high-frequency IIC clock lines, high-frequency SPI clock lines, etc., it is important to check whether instantaneous peak currents will be generated.

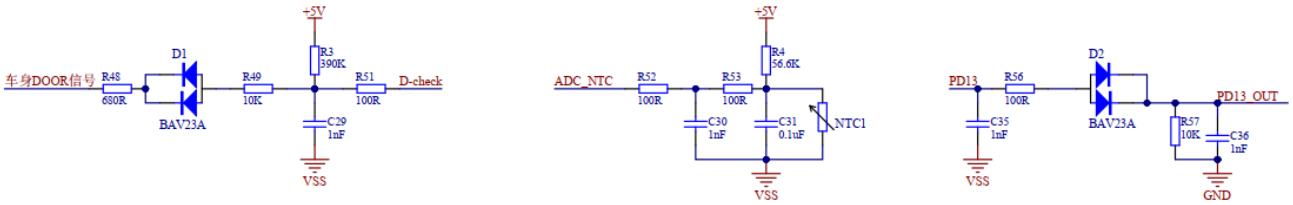
## 2.5 Connect the Input/Output signal port to a current limiting resistor in series and connect the capacitor to VSS in parallel

For Input/Output ports (e.g. ADC, external interrupts, communication interfaces, etc.), it is recommended to connect to the protective resistors in series in circuit design. The resistance value should be considered and calculated, and the theoretical maximum current should not exceed the limit parameters that the chip port can withstand; the resistors connected in series and capacitors connected in parallel should be placed as close as possible to the chip pins, and the resistors should be connected in series before the capacitors are connected in parallel. The

ground of the filter capacitor of the peripheral module must be connected to the ground that has passed through the large and small filter capacitors (VDD, VSS). As shown in Figure 5, the IO port is connected in series to a 100R resistor and connected in parallel to a 1nF capacitor.

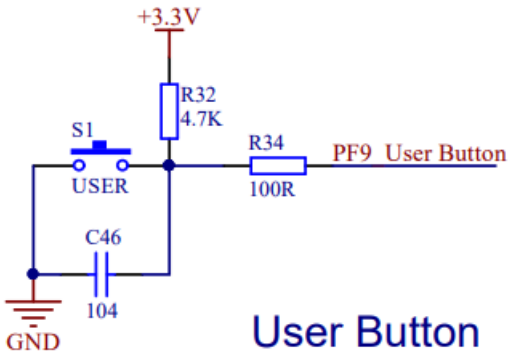
Note that in the design of PCB interconnection (similar to separating lamps from control modules, separating sensors from control modules), this series-connected resistors and parallel-connected capacitors should be placed on the PCB board of the chip. Reasonable parameters and placement positions can effectively prevent damage to the chip ports by ESD/EOS.

Figure 5 An Example of Resistor and Capacitor Connection




For button circuits, the recommendations are as follows:

Figure 6 Button Circuit




As shown in Figure 6, connect a small resistor R34 in series, e.g. 100R, in the GPIO, and place the capacitor C46 as close as possible to the button S1 when designing the PCB So that it can avoid the negative impact pressure generated by buttons.

## 2.6 IO voltage cannot be higher than VDD voltage

When the IC is not powered by VDD, but there is voltage at the IO port, this voltage will be supplied to the IC through a pull-up protection diode. Or when the IC is powered by VDD, but there is a higher voltage at the IO port than VDD, the voltage difference between this voltage and VDD will cause the pull-up protection diode to conduct, making the current flow into VDD. Under normal circumstances, IO cannot exceed 0.3V above VDD.

This phenomenon can easily cause the following hazards:

(1) Too high current will cause the clamp diode on the IO port to quickly overload and be

damaged.

(2) It will make MCU reset unsuccessfully.

(3) It will cause disorder in the chip program.

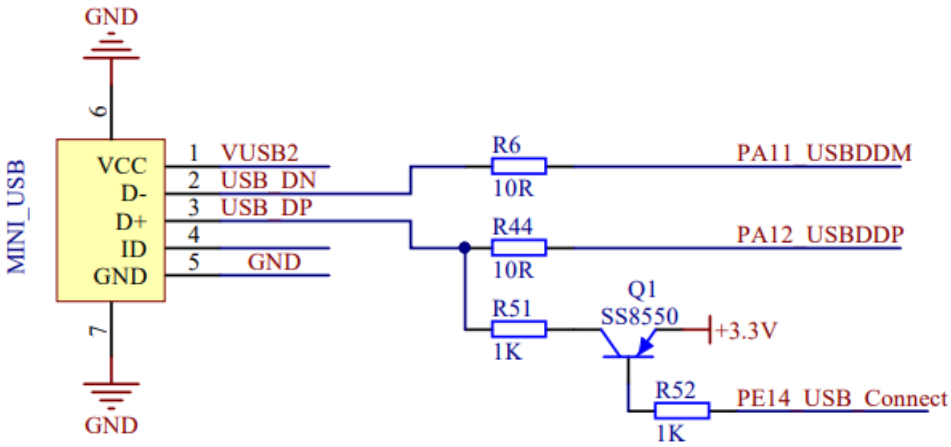
(4) A latch-up effect will result.

## 2.7 Pay Attention to Protection for Exposed Ports

For communication ports, ESD protection measures are required. A small resistor (e.g. 10R, 100R) can be connected in series on the signal line to limit the amplitude of ESD current; transient voltage suppressor diodes (TVS) can be connected in parallel on the signal line, near the interface position. It is as shown in Figure 7 Communication Circuit.

There is a hot-plugging risk in the burning port, and it should be protected by first contacting GND and then contacting IO during the connection.

Figure 7 Communication Circuit



# 3 Precautions for Software Application

## 3.1 Precautions for GPIO Operation

1. Unused GPIO ports should be set to output low level or connect an external 100Ω resistor for pull-down.

2. Different GPIO pins should avoid being configured with the same multiplexing function!

3. When the chip VDD is powered on within the range of 0V-2V, the GPIO port is in an uncertain state, and attention should be paid to the impact of unstable condition of GPIO on the stability of the post-stage drive circuit; when VDD is powered on above 2V, after the chip completes the power-on reset, the status of the GPIO port will be executed according to the program settings.

4. When the GPIO port is configured as a multiplexing push-pull output, it is recommended to connect an external pull-up resistor; when it is configured as a floating input, it is recommended to connect an external pull-up resistor or modify the software to a pull-up input, otherwise the voltage may be affected by external factors and stable levels cannot be outputted or read.

5. When Switching the I/O pin mode directly from "push-pull output high level" to "input mode", there is a level delay phenomenon. It is suggested that after the push-pull output high-level is completed, insert the push-pull low-level output or configure as open-drain pull-up output mode, and then switch to input mode. Or increase the duration of the input/output pull-down input mode (e.g. delay of 3s).

## 3.2 Precautions for Delay

When performing level inversion under software delay, the pulse width interval is unstable, e.g. for (i=0; i<1000; i++). It is recommended to achieve accurate delay through a timer.

## 3.3 RTC Precautions

Configure the automatic wakeup overload value for RTC, select wakeup output, and the period of PC13 output waveform is about 30us less than the set value. If PC13 is used to output pulses, it is recommended to use negative pulse for output.

## 3.4 BOOT pin

The BOOT pin cannot float. According to the specification requirements, the BOOT0 pin needs to be grounded when starting from Flash normally.

## 3.5 Precautions for TSC_IO Sampling

When the first I/O of each TSC group is used as the sampling I/O and the second I/O is used as the charging I/O, and the TSC_IOHCR values of the Schmitt hysteresis registers are 0xEEEEEEEE and 0xFFFFFFFF respectively, the charging time after enabled is longer than that not enabled. But under normal circumstances, the charging time after enabled is shorter than that not enabled.

When enabling TSC, it is recommended to enable the Schmitt hysteresis registers uniformly.

## 3.6 TSC_CNT6 Difference

The same TSC_CNT has significant differences in its values at different I/O rates.

When the maximum error count of TSC is set to be smaller than TSC_CNT, it will be impossible to set the flag bit of the corresponding channel.

(1) The first I/O of each group is used for electrode charging, and the second is used for sampling I/O:

I/O is configured in high-speed mode, and TSC_CNT2 and TSC_CNT6 are about 2500.

I/O is configured in low-speed mode, and TSC_CNT2 and TSC_CNT6 are about 700 or 1200.

(2) The second I/O of each group is used for electrode charging, and the first is used for sampling I/O:

I/O is configured in high-speed mode, and TSC_CNT3 is within 3000~5000.

I/O is configured in low-speed mode, and TSC_CNT3 is about 1000.

It is recommended to choose either of the following solutions:

a. I/O rate is configured as low speed;

b. Change the maximum error count setting of TSC.

## 3.7 Precautions for SPI Low-voltage Switching Polarity

Switching the SPI clock polarity at low voltage will cause invalid data 0xFF and valid data to be stored in the shift register and data register, resulting in SPI bus data exception.

When SPE(SPI_CR[6]) is 1, the value of CPOL/CPHA(SPI_CR[1]) cannot be changed. Or when changing the SPI configuration, the software will set SPE to 0 first.

## 3.8 Precautions for I2S

When I2S1 or I2S2 is configured as slave transmission mode and the clock polarity is configured to high, it will result in data misalignment.

When all pin attributes of I2S1 and I2S2 are configured as follows, normal communication can be achieved:

GPIO_Mode = GPIO_Mode_AF

GPIO_PuPd = GPIO_PuPd_UP

## 3.9 Comparator

Configure COMP1/COMP2 to extremely low power, and under the extreme input signal sources (e.g. when the period of the sine wave is too small, for example, T=13us), the COMP_OUT of

COMP1 and COMP2 will maintain a constant high-level output after outputting a small square wave band.

By modifying the mode of the comparator from extremely low power to low power, COMP_SUT can output normally.

## 3.10 PLL low-frequency output is unstable

The PLL output frequency of the chip is low (e.g. less than 24MHz) and the frequency is unstable.

When using PLL multiplication, it is recommended to first use a large multiplication coefficient to increase the frequency of the VCO, and then output at a lower frequency. For example, increase the PLL frequency to 48MHz and then divide its frequency to 24MHz through an AHB prescaler.

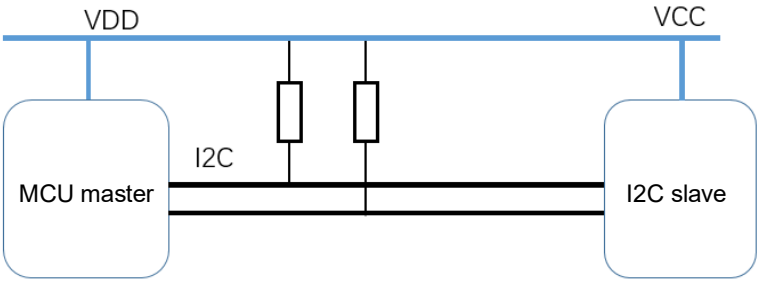
## 3.11 Precautions for I2C

In the process of sudden power failure and recovery of pull-up power supply of SCL/SDA, there is a possibility that the combination of SCL/SDA voltage and logic timing may trigger START but not STOP, resulting in the bus remaining in BUSY state. Recommended avoidance scheme:

1. The pull-up power supply of I2C must be stable to prevent the power supply from dropping too low due to instability during use. For common scenarios of I2C master-slave communication, the following hardware design is recommended:

a. The host and slave share power supply;

Figure 8 I2C Communication Circuit




b. When the host and slave cannot share power supply, it is recommended to connect the power supply of pull-up resistor to the power supply of host MCU.

2. The bus can also be released by resetting the slave. If EEPROM is used as a slave, it is impossible to reset the salve using the software, and the bus release function needs to be added to the I2C host when establishing a new communication. Due to the probability of bus locking, the bus BUSY status timeout function can be added. Combination of the two can improve the robustness of the system.

3. If the I2C device on the bus can recognize power failure, turn off the I2C module before power failure.

# 4 Precautions for Use of Simulators/Burning Tools

## 4.1 IAR compatibility

In IAR 8.30.1 version, debugging cannot be performed normally if xxM32F072VB is used, and if M0+ core is selected, debugging can be performed.

It is recommended to download the IAR chip which supports the file package (Geehy.APM32F0xx.AddOn_v1.0.0.exe), and after installation, burning and debugging can be performed.

## 4.2 Burning

When the xxT pack is used on Keil5.27 version, it cannot be burnt through AP-LINK and ULINK2.

It is recommended to use APEXMIC.APM32F0xx_DPF or keil.xTM32F1xx.DFP.2.2.0.pack.

## 4.3 ISP download

The chip may be unable to enter the DFU upgrade mode under ISP.

Consider using IAP method for DFU download; or solve related problems by migrating F072 A5 or the new version A1/A2

# 5 Revision history

Table 1 Document Revision History

| Date | Version | Revision History |
|---|---|---|
| March,2025 | 1.0 | New |

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